UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,987,694 B2
APPLICATION NO. : 10/640082
DATED : January 17, 2006
INVENTOR(S) : Lee

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 14,
Line 24-25 should read -- second word line, applying a program voltage to a third word line connected to a third memory cell transistor of the string,

Line 27 should read -- sive to applying the program voltage to the third word line --

Line 29 should read -- the first and third memory cell transistors of the serially --

Column 15,
Line 13 should read -- nel of the third memory cell transistor with a first precharge --

Line 17 should read -- connected to the third word line with a second voltage --

Column 16,
Lines 57-58 should read -- a program voltage to a third word line connected to a third memory cell transistor of the string while applying the --

Lines 61-62 should read -- the third memory cell transistor being programmed responsive to applying the program voltage to the third word line --

Line 64 should read -- the first and third memory cell transistors of the serially --

Column 17,
Line 36 should read -- of the third memory cell transistor with a first precharge --

Line 40 should read -- connected to the third word line with a second voltage --

Column 18,
Line 6 should read -- supplying a program voltage to a third word line connected to --

Line 8 should read -- the first word line is closely adjacent to the third word line --

Line 27 should read -- each of the memory cell transistors stores 1-bit data. --

Line 48 should read -- lines being closely adjacent to a third word line connected to --

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,987,694 B2
APPLICATION NO. : 10/640082
DATED : January 17, 2006
INVENTOR(S) : Lee

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 19,
Line 16 should read -- being closely adjacent to a third word line connected to the --

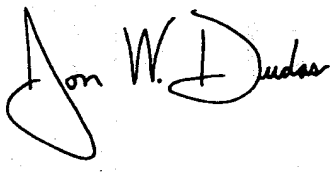
Line 18 should read -- supplying a program voltage to the third word line , wherein the --

Line 55 should read -- first word line, a decoupling voltage to a third word line --

Column 20,
Line 14 should read -- 78. The memory device according to claim 80, wherein --

Signed and Sealed this

Fifteenth Day of August, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office